C_{OSS} Loss of GaN HEMTs: Similarities and Distinctions in p-gate HEMT, GIT, Direct-drive, and Cascode HEMT

The output capacitance (C_{OSS}) loss, produced when the device's output capacitor is charged and discharged, has become a concern for GaN high electron mobility transistors (HEMTs) in high frequency applications. This work comprehensively characterizes the C_{OSS} loss of various GaN HEMTs. Their C_{OSS} loss exhibits some common dependencies, including a non-monotonic relation with the *dv/dt* (or resonance frequency), a linear relation with the on-state I_{DS}, a power-law relation with the peak V_{DS}, and little temperature dependence. In addition, their C_{OSS} losses all show minimal distinctions in a single pulse and in the steady-state switching up to 1 MHz switching frequency (f_{SW}). A common model is developed to describe the C_{OSS} loss of p-gate HEMTs, GITs, and direct-drive HEMTs, which can be expressed as:

$$P_{OSS} = f_{SW} k \left[\alpha + \beta I_{DS(max)}\right] V_{DS(peak)}^{\gamma} \quad (1)$$

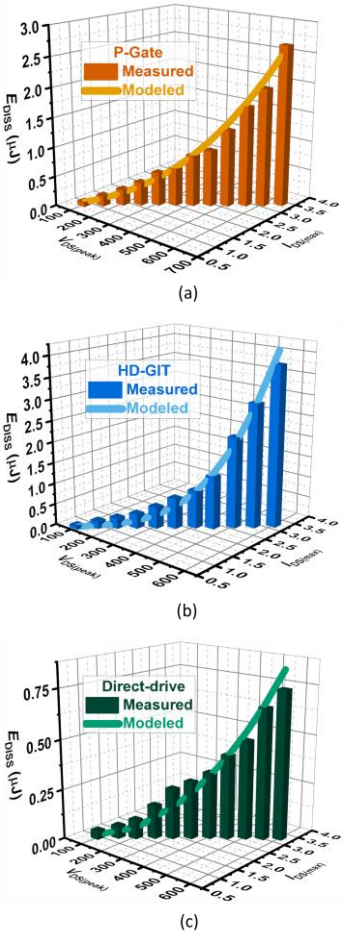

Fig. 1. Experimental data and model fitting of C_{OSS} loss for the (a) p-gate HEMT, (b) HD-GIT and (c) direct-drive HEMT.

Fig. 1(a)-(c) show the fitted E_{DISS} at various $V_{DS(peak)}$ and $I_{DS(max)}$ for all standalone E-mode and direct-drive HEMTs at a frequency of 6.78 MHz. Suitable agreement is shown between the modeled and experimental E_{DISS} results. The cascode GaN HEMT was found to have the largest C_{OSS} loss, due to two extra loss components besides the C_{OSS} loss of the GaN HEMT (E_{DISS}(GaN)), compared with other standalone E-mode and direct-drive HEMTs. These two loss components are a) the avalanche loss of Si MOSFET (E_{AVA} (Si)) and b) the Si avalanche induced GaN hard turn on loss (E(GaN_HO)). Fig. 2(a) shows the experimental loss breakdown of these three loss components, which shows a suitible agreement between the sum of them and the tested total loss of an off-shelf cascode GaN HEMT (DUT 1). The C_{OSS} loss can be significantly reduced by eliminating the Si avalanche, realized by paralleling a capacitor with the Si MOSFET in a decapsulated cascode HEMT (DUT 2), as illustrated in Fig. 2(b). Fig. 2(c) shows that a 75% decrease of C_{OSS} loss is achieved after adding the parallelled capacitor to the

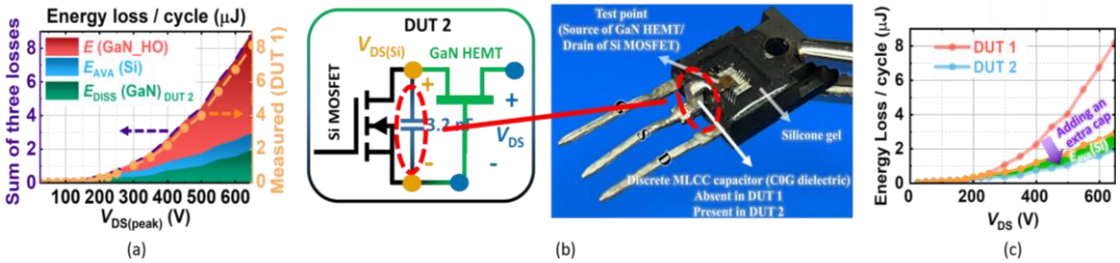

Fig. 2. (a) C_{OSS} loss breakdown for the cascode (b) Illustration and photo of DUT 2 (c) Loss comparison between DUT 1 and DUT 2

decapsulated, compared to the off-shelf cascode GaN HEMT. These results provide important references for the high-frequency application of GaN HEMTs and new insights into the physical origin of their C_{OSS} loss.