A PCB-embedded 1.2 kV SiC MOSFET Package with Reduced Manufacturing Complexity

The PCB-embedded 1.2 kV SiC MOSFET half-bridge package designed in this work targets a minimized manufacturing complexity and footprint, while also meeting the electrical and thermal performance necessary to operate in a high power density, 22 kW onboard charger (OBC). More specifically, the electrothermal viability, manufacturing complexity, and footprint size of alternative package designs with varying levels of gate- and power-loop component integration, layer counts, and trace widths were evaluated. Quantitative metrics related to PCB manufacturing complexity, such as layer and via counts, were used to determine the relative manufacturing complexity of each design alternative.

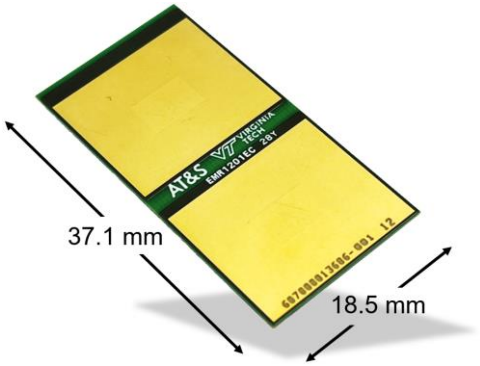

Fig. 1. The final PCB-embedded SiC MOSFET half-bridge package. The package is 0.47 mm thick.

The final package, shown in Fig. 1., was fabricated by AT&S and experimentally tested by CPES to measure its performance. Double pulse tests performed on the final package at 800 V and 25 A revealed that the low loop inductances allow the switches to achieve approximately 40 V/ns turn off dv/dt and a drain-to-source voltage overshoot of less than 5%. The selection of a non-isolated case, along with other design choices, has helped limit the junction-to-case thermal resistance ($R_{TH,JC}$) of each MOSFET to 0.074 K/W. As shown in Fig. 2., the $R_{TH,JC}$ of the package designed in this work is lower than that of a TO-247 package and a highly integrated PCB-embedded package with double-sided cooling (DSC), each of which contains the same die.

Compared to the PCB-embedded package in Fig. 2., which gave less consideration to manufacturing complexity, the PCB-embedded package designed in this work had more than 98% fewer copper-filled microvias, less than one-sixth the footprint, and half the number of copper layers. However, the package designed in this work did not achieve a smaller footprint and lower manufacturing complexity without negotiating certain tradeoffs. This package forwent DSC and gate- and power-loop component integration to reduce manufacturing complexity and footprint at the expense of optimal electrical and thermal performance. The conclusions drawn about the impact of design choices on manufacturing complexity and footprint size of PCB-embedded packages will aid in the design of PCB-embedded packages for other applications with the goal of reducing cost at scale while maintaining sufficient performance.

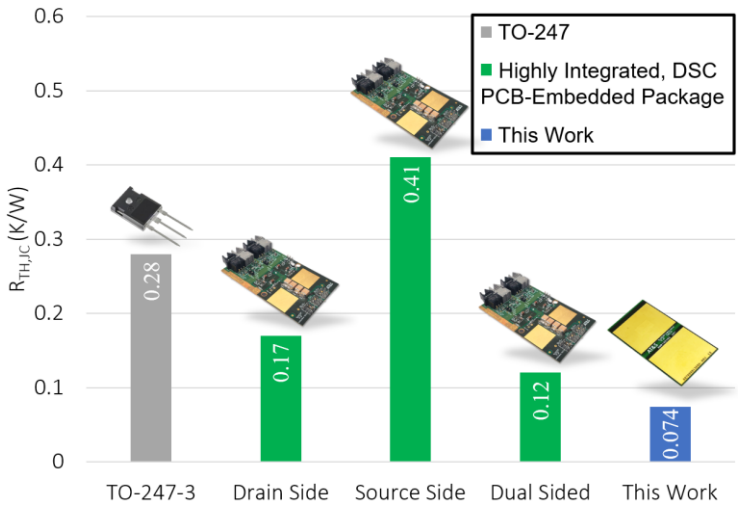

Fig. 2. Measured $R_{TH,JC}$ of a TO-247 package, a highly-integrated PCB-embedded package with DSC, and the package designed in this work