Gate Robustness and Reliability of P-Gate GaN HEMT Evaluated by a Circuit Method

The small gate overvoltage margin is a key reliability concern of the GaN Schottky-type p-gate high electron mobility transistor (GaN SP-HEMT). Current evaluation of gate reliability in GaN SP-HEMTs relies on either DC bias stress or pulse I-V method, neither of which resembles the gate voltage (V_{GS}) overshoot waveform in practical converters. This work develops a new circuit method to characterize the gate robustness and reliability in GaN SP-HEMTs, featuring 1) a resonance-like V_{GS} ringing, 2) pulse width down to 20 ns, and 3) an inductive switching concurrently in the drain-source loop. Fig. 1 shows the circuit schematics and exemplary waveforms. Using this method, the gate's switching lifetime is first obtained and characterized under hard switching (HSW) and drain-source grounded (DSG) conditions, under switching frequency (f_{SW}) at 10 kHz and 100 kHz, and at 50 and 125° C.

The number of switching cycles to failure (*SCTF#*) under each test condition can be fitted by Weibull or Lognormal distributions. The *SCTF#* shows a power law relation with V_{GS} peak value and little dependence on the switching frequency. More interestingly, the gate's lifetime is higher in HSW than those in DSG, as well as at higher temperatures. Fig. 2 shows an example of the max $V_{GS(PK)}$ under failure probability (*P*) at 63% and 0.1%, estimated by the *SCTF#* under the corresponding *P* at f_{SW} = 100 kHz, extracted from the Weibull distribution. At 125° C and 100 kHz, the V_{GS} limits for a 10 year lifetime are projected to be ~6 V and ~10 V under the DSG and HSW conditions, respectively.

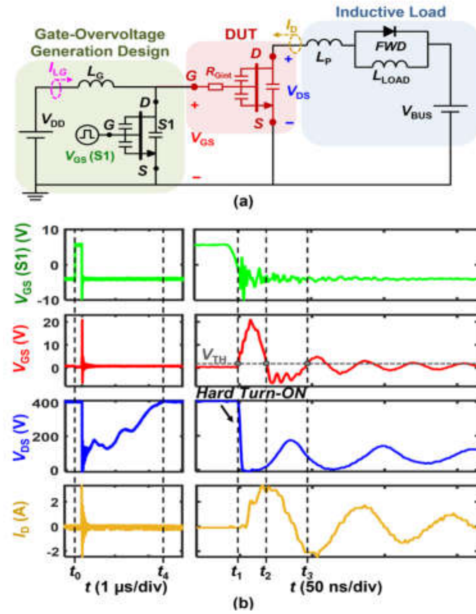

Fig. 1. (a) Schematics of the gate overvoltage test circuit in HSW condition (b) Test waveforms in the 400 V inductive HSW with PW = 20 ns and $V_{GS(PK)}$ = 21 V (Left) A whole switching cycle (Right) Zoom-in view of the V_{GS} overshoot period

The above experimental findings can be explained by the time-dependent Schottky breakdown mechanism, which is supported by the failure analysis and physics-based simulation. Finally, the device degradation behaviors are characterized under the prolonged stress of V_{GS} overshoot. The gate leakage current is revealed to be the major degradation precursor, and the degradation is confirmed to first occur at the p-GaN Schottky contact in the gate stack.

This is the first report of the gate lifetime of GaN SP-HEMTs in inductive converters, providing a new qualification method and revealing new physical insights for gate reliability and robustness in p-gate GaN HEMTs.

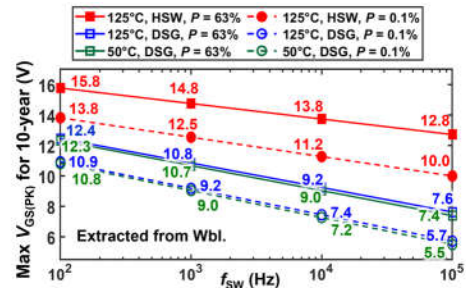

Fig.2. Projected max $V_{GS(PK)}$ for 10 year lifetime as a function of f_{SW} (100 Hz ~100 kHz) under 125°C, DSG, 125°C, HSW, and 50°C, DSG conditions, at P = 63% and 0.1%, using SCFT# at 100 kHz under the corresponding P extracted from Weibull distribution