Easy to Implement Sub-10 ns Synchronization Techniques for PEBB-based Modular Power Converters

For large-scale, PEBB-based modular power converters, high performance distributed control systems are preferred for their modularity, scalability, and flexibility. However, such distributed control systems also raise the need for minimal synchronization errors (SE) of communication networks. This work develops two sub-10 ns synchronization techniques that are easy to implement. Unlike White Rabbit-based synchronization, such techniques operate without the need for an analog PLL. The entire synchronization process is digitally executed within the FPGA, markedly reducing implementation complexity.

Fig. 1. shows the synchronization technique with a physically shared clock**.** PTP packet is generated in the main controller and sent to the PEBB controller via the communication link. Syntonization is achieved by physically sharing the clock, which means that additional fiber is needed. One main controller and one PEBB controller are connected to verify this synchronization approach. Both controllers are based on Intel/Altera MAX10 FPGA, and the physical layer for communication is ribbon cable. The FPGA local clock frequency on each controller is set to 125 MHz, and a local time counter is generated based on its own clock. With the system running for over 10 hours and 206,943 samples collected, the synchronization performance is observed. Both the latency and jitter are below 1 ns.

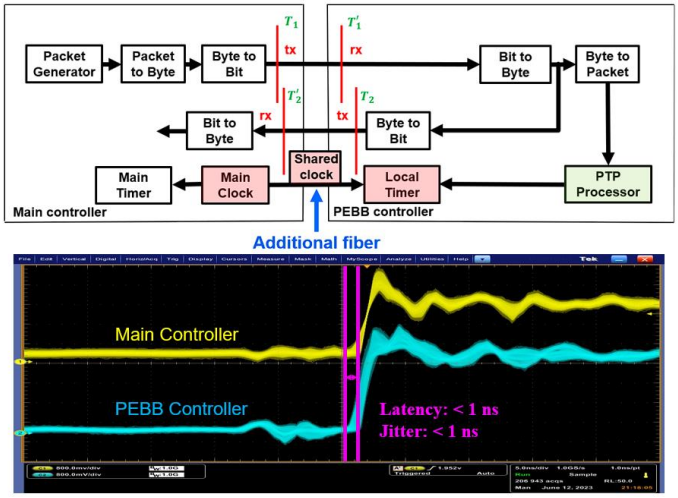

Fig.1. Synchronization technique with physically shared clock

Fig. 2. shows the synchronization technique with a recovered clock. In this approach, instead of physically sharing the clock, the PEBB controller regenerates the clock signal from the communication, removing the need for additional fiber. A VHDL-based clock and data recovery (CDR) block is implemented in the PEBB controller. The system clock is set to 200 MHz. With the system running for over 12 hours and 2,172,245 samples collected, a synchronization performance of 2.5 ns latency and 5 ns jitter is observed.

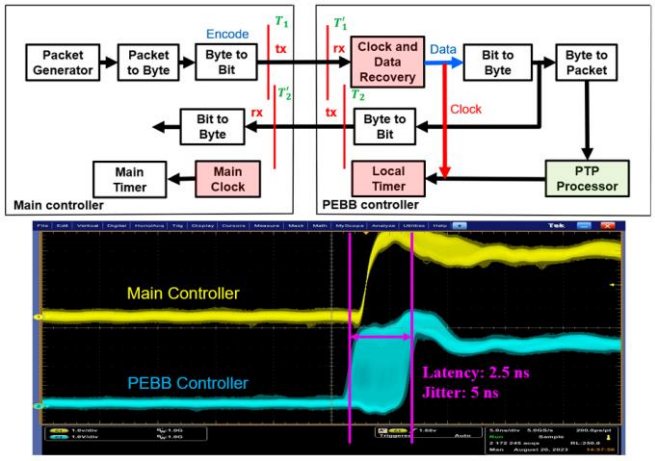

Fig. 2. Synchronization technique with recovered clock

In conclusion, two easy-to-implement sub-10 ns synchronization techniques have been designed, developed, and experimentally verified. The first technique achieves <1 ns jitter and a <1 ns latency but needs additional fiber, while the second technique achieves 5 ns jitter and 2.5 ns latency but does not need additional fiber.